DERWENT-ACC-NO: 2003-413852

DERWENT-WEEK: 200339

TITLE: Method for fabricating trench of isolation layer of flash memory device

INVENTOR: CHOI, B H; KIM, T G ; LEE, H G ; LEE, M H ; SIM, S B

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2001KR-0038409 (June 29, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2003002709 A	January 9, 2003	N/A	001	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2003002709A	N/A	2001KR-0038409	June 29, 2001

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: KR2003002709A

BASIC-ABSTRACT:

NOVELTY - A method for fabricating a trench of an isolation layer of a flash memory device is provided to prevent a substrate from being damaged and reduce a leakage current by forming trenches having the same depth in a shallow trench isolation(STI) region and a deep trench isolation(DTI) region and by more deeply etching the trench in the DTI region.

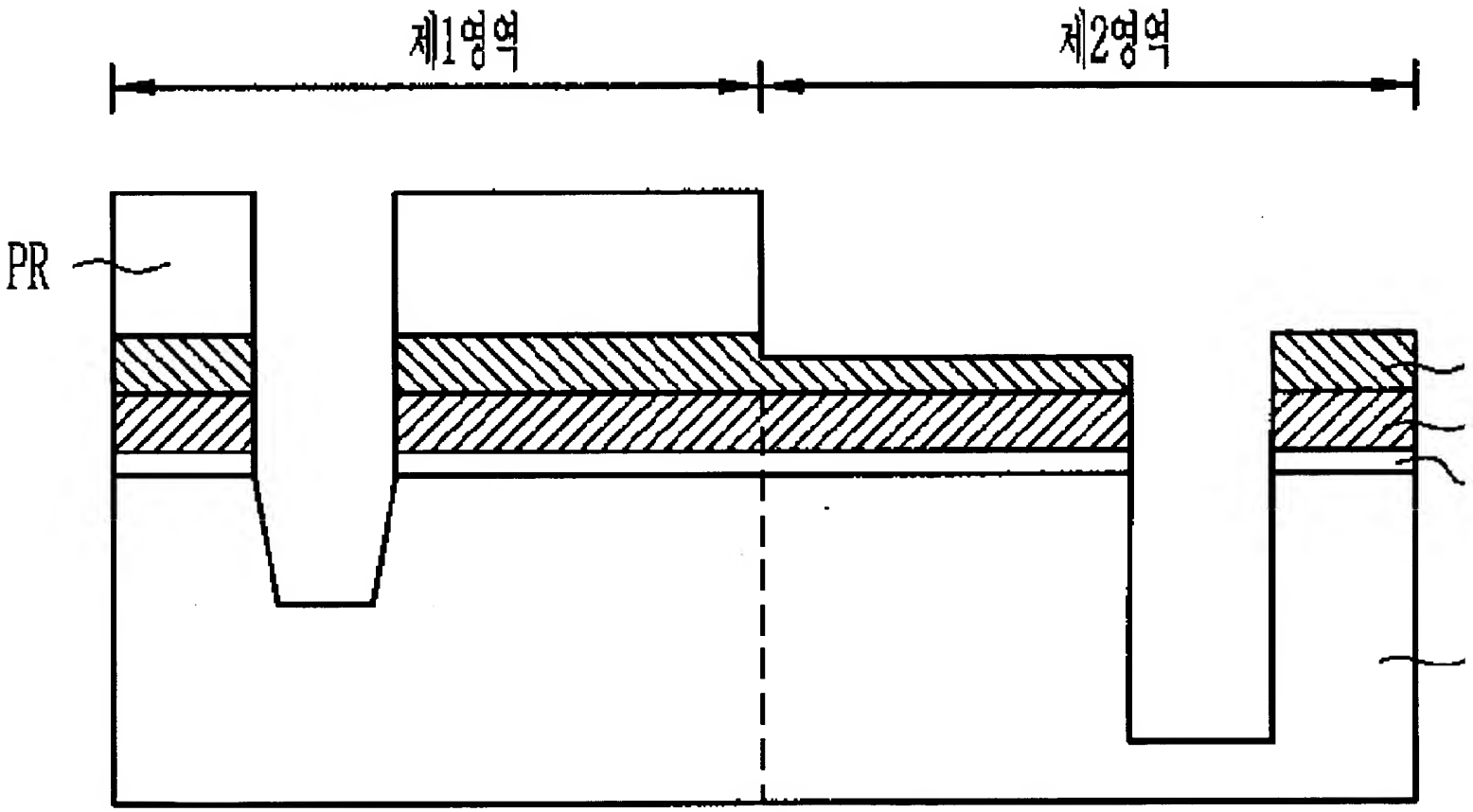
DETAILED DESCRIPTION - A pad oxide layer(210), a pad nitride layer(220) and the first oxide layer are sequentially formed on a semiconductor substrate(200) in which the first and second regions are defined. The trenches having the same depth are formed in the first and second regions. The trench formed in the second region is more deeply etched. A well oxidation process is carried out.

CHOSEN-DRAWING: Dwg.1/10

DERWENT-CLASS: L03 U11 U13 U14

CPI-CODES: L04-C07E; L04-C12C;

EPI-CODES: U11-C08A2; U13-E03; U14-A01;


제1영역
제2영역
PR